The concept of hierarchical design: the views of computer science and engineering students

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This paper focuses on the investigation of the views of Computer Science and Engineering Students (CSES) regarding the concept of hierarchical digital design within the context of Logic Design. At the end of a one-semester course in hierarchical design, CSES participated in final exams where they were asked to 'design an 11-Bit Full Adder (FA) using blocks of 4-Bit FA'. Two hundred CSES participated in these exams and their papers were studied in terms of their conceptions of hierarchical design. The subsequent data analysis reveals that these students have serious difficulties with the previously mentioned concept. These difficulties mainly centred on the operation of both a 1-Bit FA and a 4-Bit FA as well as basic rules of logic design and hierarchical design. Taking into account these difficulties, appropriate teacher interventions could be designed. In particular, an awareness of these difficulties is essential if a learning context is to be designed that takes into consideration modern constructivist and social views of learning. In this paper, proposals for the design of such contexts are also reported.

Keywords

Hierarchical digital design, Logic design, Students' Misconceptions, Tertiary Education.

1. Introduction

The concept of hierarchical design is essential for Computer Science and Engineering Students (CSES) to grasp as it is a significant concept in the development of software and hardware systems. The use of top down hierarchy involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the sub-modules has reached a suitably comprehensible level of detail [1] (p.239). The concept of hierarchical design is used in a variety of courses included in the curricula of Computer Science and Engineering departments. In this paper, emphasis is placed on the use of bottom-up hierarchical design in hardware courses and especially in Logic Design (LD).

In Logic Design, the first level of hierarchy consists of a number of Logic Gates used to implement basic Boolean functions such as 1-bit Full Adder (1FA), the whole configuration of the aforementioned logic gates creating a new entity, the 'module', in our example: 1FA-module [2]. As each 1-Bit FA consists of two Half-Adders, understanding the operation of 1-Bit FA pre-supposes understanding the operation of Half-Adder in terms of its Truth-Table and its diagrammatic configuration using logic gates [2]. At the second level, the 1-bit Full Adder is used as a basic building block to construct one 4-bit Full Adder (4FA). This 4FA can easily be constructed by appropriately connecting four 1FA-modules. At the third level, a number of 4FAs could be used to construct FAs with a variable number of bits eg. 7-bit, 12-bit, 32-bit, etc. The FAs constructed at this level can be directly used as building blocks in an ALU (Arithmetic Logic Unit) in a microprocessor (MCPU).

Understanding hierarchy within the context of LD means understanding the previously mentioned 3-level hierarchy. However, this implies the formation of a kind of hierarchical thinking, an abstract, synthetic and progressive mental process that serves to form a sophisticated, high level idea using a multi-layered hierarchy of less complicated ones ([3], [4]). At each level of this hierarchy, simple ideas are connected to produce more complicated ones. Hierarchical thinking implies analytic and synthetic skills and, in some cases, innovation capabilities [5]. Hierarchical thinking is essential for the learning of many CS concepts such as Computational Algorithms, Operating Systems, Networks, etc.

Learning hierarchical design within the context of LD is not an easy task. Traditional approaches to teaching at Tertiary level emphasize lecturing for content presentation and laboratory experience for the consolidation of the content presented. Despite this fact, students' misconceptions about the hierarchy used in LD still exist. Contrariwise, modern constructivist and social views of learning emphasize knowledge as an active, subjective and constructive activity in a context providing multiple aids and tools ([6], [7], [8]. Especially in Computer Science and in Engineering Education (EE), these modern theories have been widely accepted. It is worth noting that, in terms of teaching systems' design in EE, various approaches have been proposed. These approaches acknowledge the role of practical, laboratory team work, project engagement, real design of specific products and use of appropriate computer simulations/robots as well as the correcting of incomplete design solutions ([9], [10], [11], [12], [13], [14]).

In our attempt to help CSES to learn the concept of hierarchical design within the context of LD, we decided to investigate their main misconceptions. Using students' mistakes as a basis for the preparation of appropriate teaching and learning settings in Tertiary education is acknowledged by modern constructivist learning theories ([15]). However, studies investigating CSES' approaches to hierarchy used in LD have not yet been reported. In the following section of this paper, the context of the previously mentioned study is presented, followed by an analysis of the data that emerged. Subsequently, these results are discussed and implications for teaching are drawn.

2. The Context of the Study

This study focuses on the approaches of CSES to the hierarchical design used in the implementation of hardware systems, in particular the design of 11-bit Full Adder using blocks of 4FAs. This study was carried out at the Department of Computer Engineering and Informatics, Patras University, Greece. The data from this study consisted of CSES's written documents (200 documents) from final exams taken after their participation in a one-semester course entitled 'Logic Design I". During this course, CSES attended lectures on the concept of digital design and hierarchical digital design, the use and operation of 1-bit and 4-bit FAs as well as blocks of 4FAs and the appropriate connection necessary to form more complicated FAs. To make better sense of the theory presented during these lectures, CSES were provided with various specific examples of hierarchical design. Students did not have any prior knowledge in the domain before entering this course. However, it is worth noting that the ratio of students to professors was about 280/1 and also that these students could sit the final exams without having attended any of the learning activities organized by the professor during the course. In fact, no more than 30% of the enrolled CSES usually participate in the class work. In addition, as the number of teaching assistants and the lab-rooms are limited, the related laboratory exercises are performed in the next semester.

In these final exams, CSES were asked to: 'implement the diagrammatic representation of an 11-bit FA, using blocks of 4FA'. The data were analyzed according to the following criteria: a) Use of the correct number of 4FAs and connecting them appropriately, b) Initialization of the circuit and c) use of explicatory comments. Next, the CSES approaches - including their misconceptions and difficulties - that emerged from analysis of these data were classified into the categories presented in the following section together with statistical data.

3. Data analysis

3.1. The correct solution to the given problem

CSES approaches to the diagrammatic representation of a 11-bit FA using blocks of 4FA were classified, taking into account the basic steps needed to arrive at the correct solution to this problem. This step-by-step correct solution, presented in Figure 1, is as follows:

A. Use of the correct number of 4FAs and connecting them appropriately: a) Use of three 4FAs, b) correct connection of these three 4FAs: this means that the Cout output of the first 4FA must be connected to the Cin input of the second FA and so on, c) for each 4FA: correct arrangement and naming of the 8 inputs which represent the two four-bit parts of numbers A and B. For example, for the first 4FA we have (A3, A2, A1, A0) and (B3, B2, B1, B0) as inputs for the appropriate pins, d) correct arrangement and naming of the 4 outputs which represent the summation of A and B. For the second 4FA, the outputs (S7, S6, S5, S4) are the sum of (A7, A6, A5, A4) and (B7, B6, B5, B4) plus the appropriate **carry input.**

B. *Initialization of the circuit*: a) initialization of the Cin input as zero for the first 4FA, b) Initialization of A12 and B12 as zeros, c) as a result the Cout of the 11FA appears in S11 pin and the Cout of the third 4FA is always zero.

C. *Use of explicatory comments:* Comments must be used to provide evidence for the diagrammatic solution given.

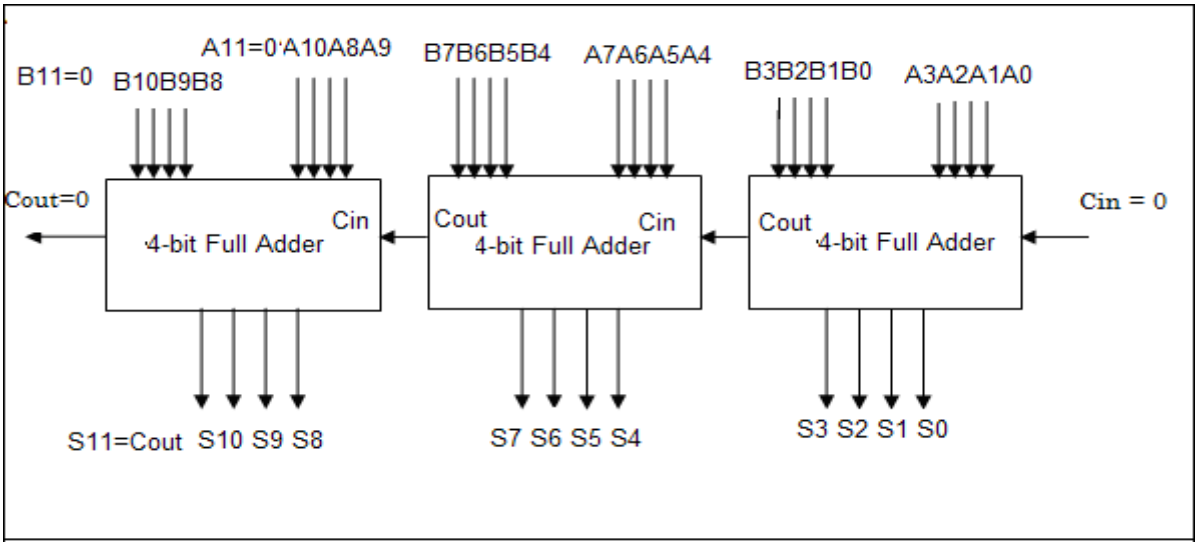
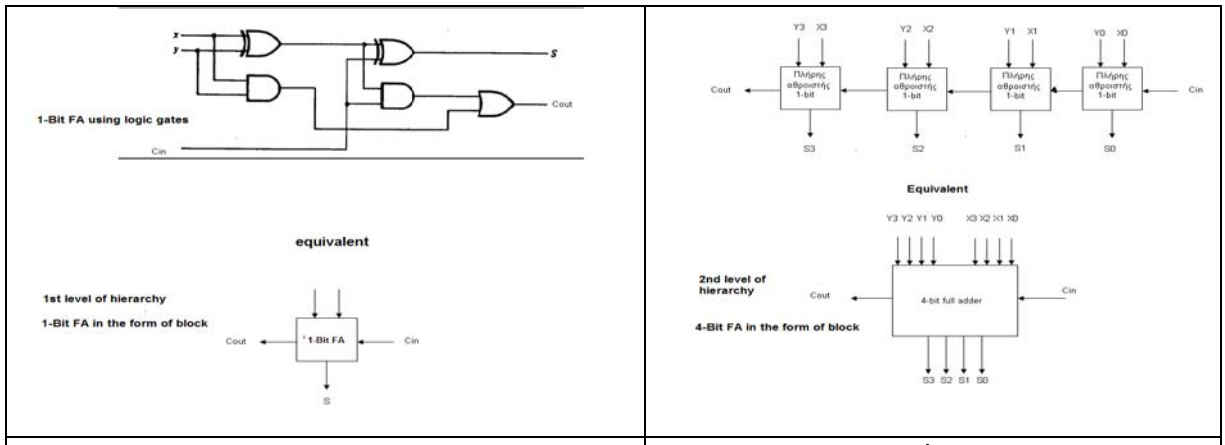


Figure 1 Diagrammatic representation of an 11-bit FA using three blocks of 4FAs

3.2. Background knowledge for the understanding of hierarchical design

Understanding of hierarchical design implies understanding a 3-level hierarchy. At the first level, learners have to understand the structure of 1-Bit FA (see Figure 2a).

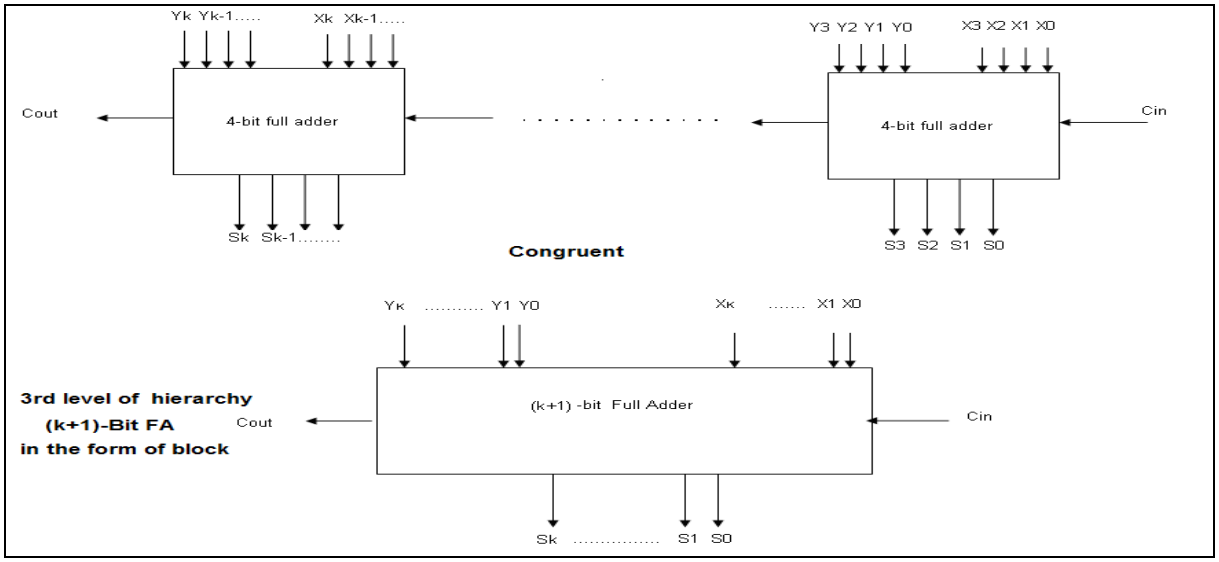
Figure 2 First and second level hierarchy



a b

At the 2nd level, students have to understand how four 1-Bit FAs are connected to produce a block of a 4-Bit FA (see Figure 2b). At the third level, students have to understand the synthesis of (k+1)-Bit FA as a block consisting of various 4FAs (see Figure 3).

Figure 3 Third level hierarchy



3.3. Categories of CSES' approaches to the diagrammatic representation of an 11FA

From the data analysis, fourteen categories of CSES approaches to the given problem were formed and these are presented in Table 1 (N = number of CSES following each specific approach and Per = Percentage). These approaches were interpreted in terms of the knowledge needed in order to perform them.

Computer Science and Engineering Students' approaches to the construction of an 11-bit FA					
Categories	N	%	Categories	N	%
C1: No attempt	26	13	**C3. Use of 2-bit-like FA instead of 4FAs**	10	5
C2. Use of 1-bit Full Adder (1FA)	16	8			
Use of 4-Bit FAs					
C4. Correct use of three 4FAs	17	8.5	**C10**. Combination of (C7, C6, C5)	8	4
C4.1. Correct but complicated initialization of inputs A11 and B11	2	1	**C11.** Design of a 12-bit FA instead of an 11-bit FA	6	3
C4.2. Correct but complicated initialization of input A11	1	0.5	**C12.** Use of 4FAs and logic gates	17	8.5
C5. Non-initialization of Cin	15	7.5	**C13.** Inverse design direction	7	3.5
C6. Non-use of comments	11	5.5	**C14**. Wrong input and output correspondence for 4FAs	9	4.5
C7.Confusion of the logic operation of the last 4FA	15	7.5	**C15**. Wrong design and connection of 4FAs	3	1.5
C8. Combination of (C7, C5)	26	13	**C16.** Wrong design of 4FAs	5	2.5
C9. Combination of (C7, C6)	5	2.5	**C17**. Use only natural language to loosely describe the solution	1	0.5

Table 1 Categories of CSES approaches to the diagrammatic representation of an 11FA

C1: *No attempt.* A significant percentage of CSES (13%) did not attempt any approach to the given problem. It seems that they had insufficient understanding of the topic.

C2. *Use of 1-bit Full Adder (1FA).* Students who performed this strategy (8%) correctly connected eleven 1-Bit FA. They did not make any explicatory comments. By taking this approach, these CSES seemed to have sufficient knowledge of digital design but inadequate knowledge of hierarchical design.

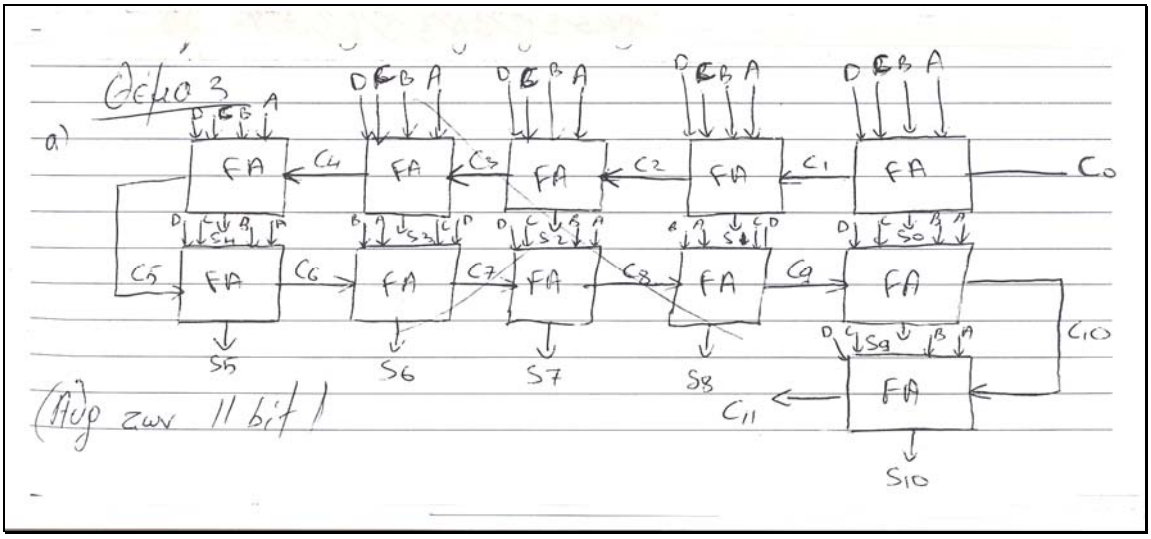


Figure 4 Example of CSES' attempts to design an 11-Bit FA that fall into category C3

C3. *Use of 2-bit-like FA instead of 4FAs*. Here, as well, some students (5%) connected eleven blocks consisting of four individual 1-bit inputs (A, B, C, D), one carry input (Co), one

carry output (C1) and only one output (So) for the sum (see Figure 4). Moreover, they did not make any explanatory comments. By taking this approach, these CSES appear to be confused about the operation and description of 1-Bit FA, 2-bit FA and 4-Bit FA. Indeed, these students used a 2-Bit-like FA with only sum output instead of a 4-Bit FA.

Use of 4-Bit FAs

C4. Correct u*se of three 4-Bit FAs.* A small percentage (8.5 %) of CSES correctly faced the given problem (as diagrammatically shown in Figure 1 and described in the previous section), i.e. the use of three 4-Bit FAs, initialization of inputs and explanation of outputs as well as use of comments. These students seemed to understand the concept of hierarchical design and also: a) the operation and description of the basic 1FA as well as that of the 4FA, b) the correct use of the carry input (Cin) and c) the correct initialization of unused inputs. Students also used alternative approaches, which are presented below.

C4.1. *Complicated initialization of inputs A11 and B11.* Students who performed this approach (1%) put an inverter with input one in each of these inputs, instead of initializing A11 and B11 to zero. It is worth noting that this approach is correct but inefficient.

C4.2. *Complicated initialization of input A11*. Some students (0.5%), realized the initialization of A11 to one, resulting in the transfer of the carry out of the 11-Bit FA from S11 to Cout of third 4-Bit FA. These students constructed a correct but complicated solution to the given problem.

However, it is worth noting that the rest of the students (64 %) incompletely used the blocks of 4FAs to solve the given problem. Student problems fall into the following categories:

C5. *Non-initialization of Cin*. This approach was taken by a considerable percentage of students (7.5%) and it is similar to that previously mentioned (C4) with the exception of the Cin initialization. Neglecting the initialization of Cin can be detrimental to the operation of addition.

C6. *Non-usage of comments*. Students who fall into this category (5.5%) faced the given problem in the same way as those included in C4, but did not report the appropriate comments. In our view, this implies a meaningless pictorial approach and also problems with a deep understanding of the topic.

C7. *Confusion of the logic operation of the last 4-Bit FA*. A significant percentage of students (27%) seemed to ignore the operation of the last 1-Bit FA included in the third 4-Bit FA. In fact, they transfer the carry out of the eleventh 1-Bit FA to Cout of the twelfth 1-Bit FA instead of S11. In our view, this means that these students have problems with the understanding of the second and third levels of hierarchy. It is worth noting that some of those students (13%) also failed to correctly initialize Cin (category C8), some others (2.5%) also left out the appropriate comments (category C9) while there were a few (4%) who combined all three of the above (category C10).

C11. *Design of a 12-bit FA instead of an 11-bit FA.* Students who took this approach (3%) used three 4FA to form a 12-Bit FA instead of an 11-Bit FA. They also did not make any explicatory comments. These students seemed to understand the general context of hierarchical design but not its essential details in terms of the correct usage and initialization of the third 4-Bit FAs (failed to initialize A11 and B11 inputs).

C12. *Use of 4-Bit FAs and logic gates*. Here, a considerable percentage of students (8.5%) used two 4-Bit FA and unsuccessfully tried to form the required extra 3-Bit FA using logic gates (see Figure 5). By realizing this solution, students reveal problems with the concept of hierarchical design and the operation of both 1-Bit FA and 4-Bit FA as well as basic design using logic gates.

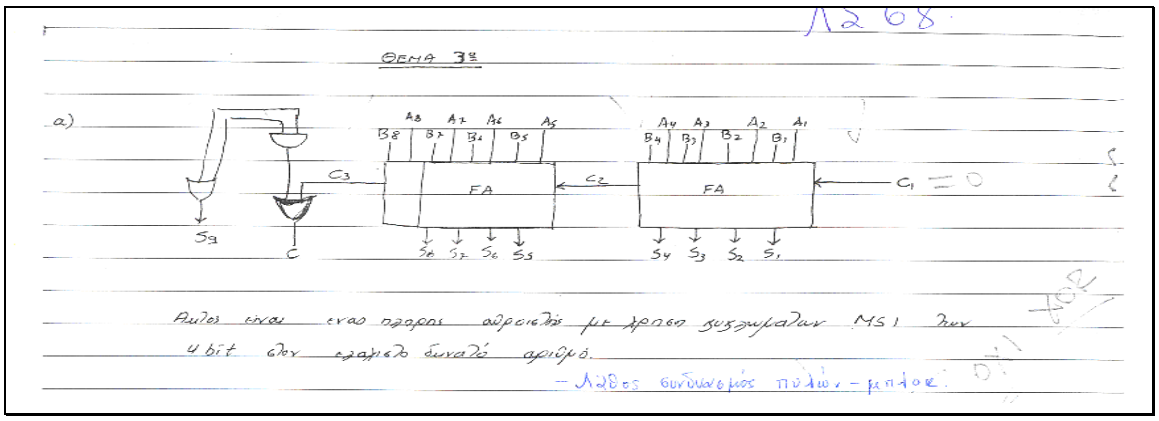


Figure 5 Example of CSES' attempts to design an 11-Bit FA by using 4-Bit FAs and logic gates

C13. *Inverse design direction*. Here, students (3.5%) designed the circuit in reverse order (from left to right). They also made the same mistakes as in category C7. These students seemed to ignore the weight of each binary digit in binary numbers and the correspondence between the real binary numbers and the circuit.

C14. *Wrong input and output assignment for 4-Bit FAs*. Here, students (4.5%) connected the three 4FA and initialized Cin and A11, B11 inputs to zero. However, they put the same numbers A7,…,A0 here as inputs in every 4FA, and also the same outputs S3…S0 (see Figure 6). The circuit produced does not operate in any manner; logically or electrically. Students who performed this approach seemed to ignore all basic rules of digital logic and also all levels of hierarchical design. On the whole, this diagram appears to assume a total lack of background knowledge.

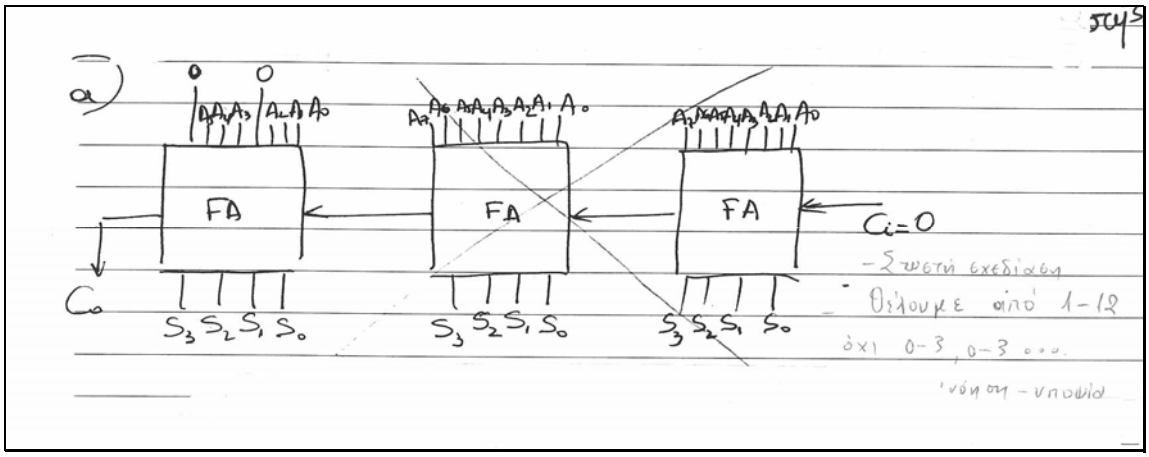


Figure 6 Example of CSES' attempts to design an 11-Bit FA using the approach fall into category C14

C15: *Wrong design and connection of 4-Bit FAs.* These students (1.5%) used three 2-Bit FA with 1-Bit sum output connected cascadingly and also using a carry output from the first to

the second and from the second to the third. There is no carry input for these adders. Finally, they used an OR gate for the summation of the three 1-Bit outputs of the three 2-Bit FA plus the carry output of the third 2-Bit FA (see Figure 7). These students seemed to confuse the 2-Bit FAs with 4-Bit FAs. They also ignored the operation of any kind of FA as well as all basic rules of digital logic and also all levels of hierarchical design.

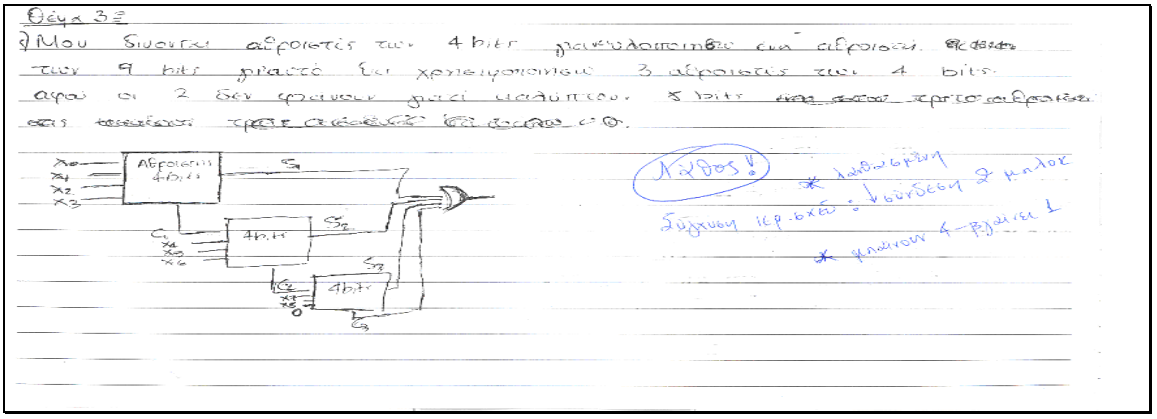


Figure 7 Example of CSES' attempts to design an 11-Bit FA using the approach fall into category C15

C16: *Wrong design of 4FAs.* Here, students (2.5%) used 1-Bit instead of four-bit outputs in every 4-Bit FA. They also omitted the twelfth, most significant bit of the operands. In addition, they did not initialize the Cin and also did not make any comments (see Figure 8). It is worth noting that the circuit produced does not operate in any manner; logically or electrically. These students also seemed to ignore all basic rules of digital logic and also all levels of hierarchical design.

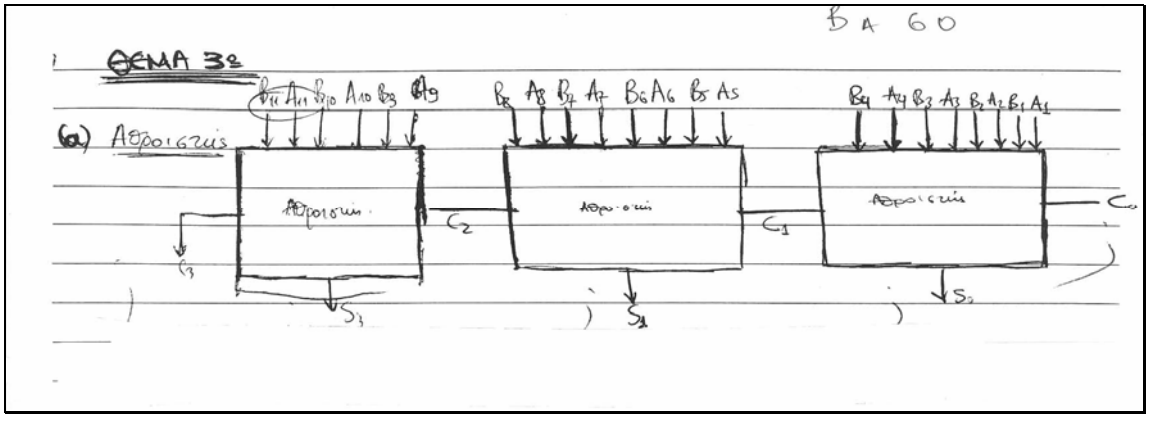


Figure 8 Example of CSES' attempts to design an 11-Bit FA using the approach fall into category C16

C5. *Use only natural language to loosely describe the solution.* Here, ,one student (0.5%) wrote a primitive internal description of the given 4-Bit FA.

3. Discussion

A first glance at the results of this study reveals that CSES present serious difficulties with hierarchical design. In fact, only a small percentage of these students successfully designed an 11-Bit FA using blocks of 4FAs whereas a considerable percentage of them seemed to fail to make sense of hierarchical design. In fact, some of CSES seemed to make no sense

at all of the fundamentals of LD (Category C1), others (Category C2) seemed not to understand the levels of hierarchical design, while the remainder (Category C3) seemed to confuse the 4-bit FA with a 4 input circuit equivalent to a 2-bit FA. Despite the fact that the majority of CSES used blocks of 4FAs in their constructions, only a small percentage used these blocks in an appropriate manner. Here, it is worth noting that about one-in-three students seemed not to understand the second and third levels of hierarchy as they ignored the operation of the last 1-Bit FA included in the third 4-Bit FA and transferred the carry out of the eleventh 1-Bit FA to Cout of the twelfth 1-Bit FA instead of S11. It is also remarkable that about one-in-five CSES did not appropriately initialize the Cin input, which means that they possibly did not understand the basic concept of LD (that every input in a logic circuit must have a digital value). Small scale misconceptions were also revealed, including design of a 12-bit FA instead of an 11-bit FA, inappropriate initialization of inputs A11 and B11 and wrong 4FA input and output correspondence. In addition, some CSES appeared to be unable to make comments about their solutions, while others appeared to possess a kind of 'design dyslexia', performing inverse designs.

In our attempt to interpret these results, we must stress that the student/professor ratio is very high (too many students per teacher). Moreover, the staff and labs for practical education in hierarchical design are inadequate. Furthermore, attendance on this course is not obligatory. In addition, students are not provided with obligatory projects, exercises, mid terms and home-work. In fact, CSES do not have any practical experience of hierarchical digital design and consequently they lack opportunities to put their approaches into practice. Taking into account all the above, we propose appropriate standards and a constructivist teaching approach to hierarchical LD and these are presented in the next section of this paper.

4. Implications for teaching

Exploiting the results of this study, and bearing in mind social and constructivist views of learning, we propose the active involvement of CSES in their learning of hierarchical design. It is also considered appropriate to assign them the responsibility to work in teams in order to complete interesting projects aimed at the design of specific useful products. The use of appropriate simulations to to help students detect any problems in their constructions is also considered significant. Furthermore, the parallel involvement of students in the laboratory is essential if they are to be able to connect theory with real practice. In fact, in the laboratory, CSES can see the results of their paper and pencil attempts and subsequently correct their mistakes. In addition, it is considered critical that students engage in correcting papers including the most serious failures of hierarchical design reported above. Finally, it is worth noting that, to realize all this work, it is essential to increase the number of both faculty members and staff in this domain of knowledge.

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